A Ka-band Down Converter IC in 65-nm CMOS for LEO-Satellite Payloads

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***Abstract*—A Ka-band down-converter integrated circuit (IC), implemented in a 65-nm CMOS process, is presented for Low Earth Orbit (LEO) satellite communication payloads. The proposed single-chip solution integrates the complete RF, IF, and LO stages and employs an in-phase/quadrature (I/Q) architecture for image rejection. In the LO path, a transformer-based quadrature coupler is compactly implemented, offering low insertion loss. A passive fourth-order low-pass filter (LPF) is employed for channel selection and spur rejection, and its gain-peaking feature is exploited to enhance wideband IF performance. Simulation results show that the chip operates over the 27.5-30.5 GHz RF band, achieving a peak conversion gain of 14.5 dB and a minimum noise figure (NF) of 8.4 dB. The total chip area, including pads, is 890 μm by 880 μm with a total power consumption of 46.6 mW.**

***Index Terms*—Frequency converter, RF transceiver, satellite communication, low-pass filter, mixer, CMOS RFIC, Ka-band**

I. Introduction

Low Earth Orbit (LEO) satellite communication is emerging as a next-generation technology that offers wide coverage and high-speed data transmission. In the millimeter-wave (mmWave) bands, phased-array systems with multiple antennas and beamforming techniques are promising solutions to overcome severe path loss [1]. Following the beamformer IC in such systems, a frequency converter is required to down-convert the received RF signal to an IF signal. To minimize size, weight, and power, it is essential to achieve a high level of integration by incorporating all the RF, IF, and LO paths into a single chip [2]. This work presents a fully integrated Ka-band down-converter IC designed to interface with a preceding phased-array IC.

II. Frequency Down-Converter Architecture

Fig. 1 illustrates the block diagram of the proposed fully integrated down-converter, fully integrating RF path, LO generation and distribution path, and IF signal processing path. The circuit adopts an I/Q architecture, which enables image rejection and provides flexibility for channel-specific calibration in subsequent digital processing.

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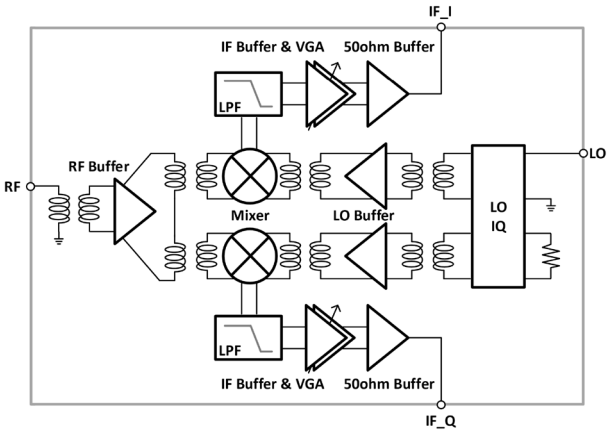

Fig. 1. Block diagram of the proposed frequency down-converter.

In the LO path, quadrature signals are generated using a transformer-based coupler. While RC polyphase filters exhibit significant insertion loss, the transformer-based coupler achieves superior loss performance [3]. Although transformer-based couplers can be area-intensive at lower frequencies, this drawback is alleviated at mmWave frequencies due to frequency scaling. Fig. 2 presents the layout and EM-simulated results of the designed transformer coupler. The compact coupler occupies an area of 170 μm $\times$ 100 μm and achieves an insertion loss of 0.6 dB, a phase error of less than 1.1°, and an amplitude error below 1 dB at an LO frequency of 25 GHz.

The IF stage integrates a passive fourth-order low-pass filter (LPF) composed of inductors and capacitors. This LPF functions as a channel-selection filter, suppressing out-of-band spurs and wideband noise at the mixer output. In addition, it is designed to exhibit intentional gain peaking near the passband edge, which compensates for high-frequency gain roll-off in the IF amplifiers and thereby extends the IF bandwidth. To maximize integration density and reduce chip area, the IF amplifiers are designed with resistive and active loads, eliminating the need for large on-chip inductors. The LPF's gain-peaking characteristic enables this area-efficient inductorless design while maintaining wideband IF performance.

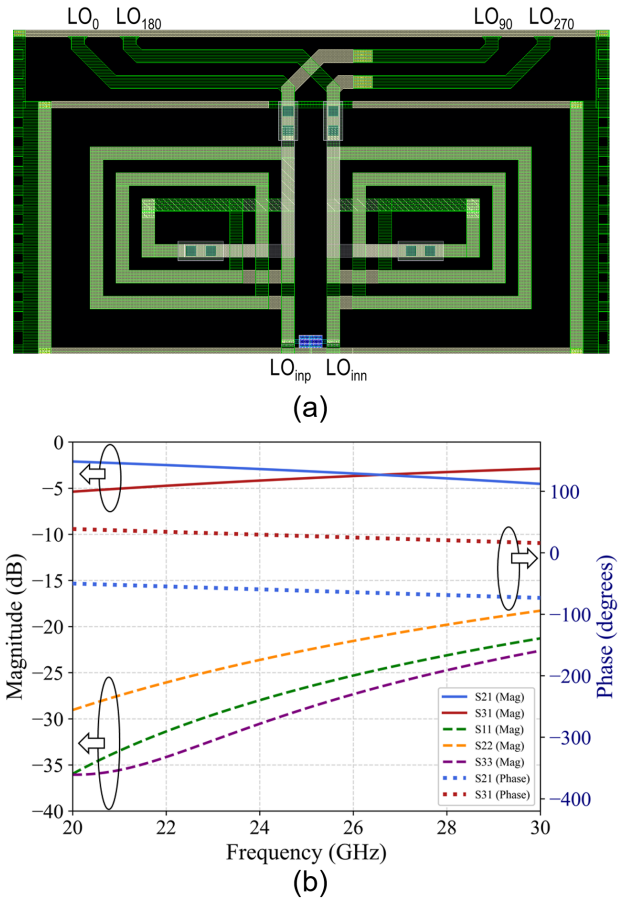

Fig. 2. (a) Layout and (b) EM-simulation results of the transformer-based coupler.

III. Simulation Results of the Down-Converter IC

The proposed down-converter IC is designed by a 65-nm CMOS process. Fig. 3 shows the layout of the chip, which occupies 890 × 880 μm^2, including all pads. The total power consumption is 46.6 mW from a 1-V supply voltage.

Fig. 4. (a) presents the simulated S-parameters with a fixed LO frequency of 25 GHz. The peak conversion gain is 14.5 dB, and the 3-dB bandwidth covers from 27.5 GHz to 30.5 GHz, with significant rejection of out-of-band signals. The input return loss (S11) is better than −8 dB across the operating band. Fig. 4. (b) shows the simulated noise figure (NF) and the conversion gain versus IF frequency. The 3-dB IF bandwidth of the conversion gain covers from 1.4 GHz to 5.7 GHz. At 4 GHz, the design achieves a minimum NF of 8.4 dB.

IV. Conclusion

A fully integrated Ka-band down-converter IC is presented in a 65-nm CMOS process for LEO satellite applications. The proposed IC integrates all RF, IF, and LO functional blocks on a single chip and interfaces with a preceding phased-array IC. A wideband IF performance is achieved by employing a passive LPF with gain peaking. Furthermore, high integration

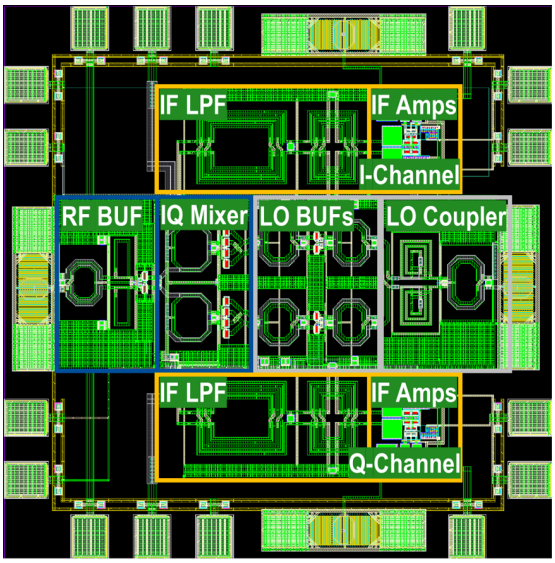

Fig. 3. Chip layout of the proposed down-converter IC.

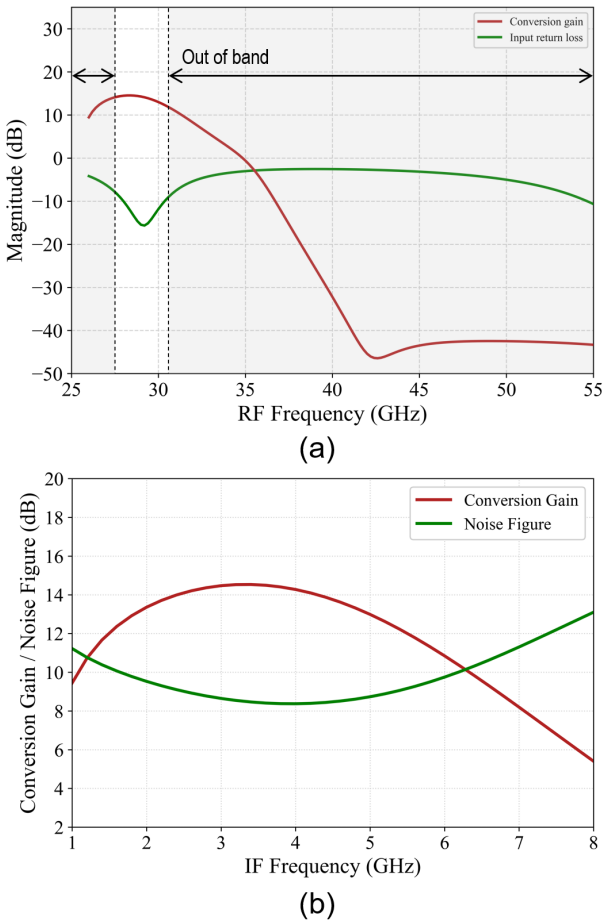

Fig. 4. Simulated performance: (a) conversion gain and input return loss versus RF frequency, and (b) conversion gain and noise figure versus IF frequency.

density is enabled by the area-efficient inductorless IF amplifiers and a compact transformer-based LO quadrature coupler. The simulated wideband IF performance and high integration density validate this design approach, offering competitive performance to other frequency converter ICs [4]–[7].

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