Enhanced Thermal Performance of RF Amplifiers via Manifold Microchannel with Porous Structure

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Abstract— High-power RF amplifiers, such as GaN high-electron-mobility transistors (HEMTs), generate intense local heat fluxes in the active device region, which can degrade electric performance. Conventional indirect cooling is limited by thermal resistances, making it difficult to manage localized hotspots efficiently. In this work, we evaluate an embedded manifold microchannel cooling structure designed for direct heat removal from the backside of a GaN-on-SiC HEMT device. Three-dimensional computational fluid dynamics (CFD) simulations of the baseline microchannel configuration were performed to quantify thermal resistance, pressure drop, and coolant flow effects. The results show a significant reduction in thermal resistance. In parallel, we present a fabrication concept for integrating a porous metal insert into the microchannel to enhance heat transfer area and uniformity. This approach is broadly applicable to high-power RF components, offering a path toward improved thermal performance, compact packaging, and operational stability.

Keywords—Thermal management, High-power RF amplifier, GaN HEMT, Direct Cooling, Manifold microchannel

I. INTRODUCTION

High-power RF amplifiers(HPAs) are widely used in communication, radar, and electronic warfare systems, where high output power and efficiency are critical. GaN HEMTs, in particular, offer high breakdown voltage, high electron mobility, and superior power density, enabling compact and efficient amplifier designs. However, under high-power operation, localized heat flux in the active device region can create severe thermal gradients. These gradients reduce carrier mobility, lower breakdown voltage, and ultimately degrade RF gain, PAE, and long-term device reliability.

Conventional thermal management structures primarily rely on indirect cooling methods, where the device is thermally coupled to a heat sink through a thermally conductive interface material. However, these indirect approaches have limitations in handling high local heat fluxes due to intrinsic conductive thermal resistance. To overcome these challenges, studies have begun exploring direct cooling structures for improved thermal performance. Ditri et al. [1] demonstrated enhanced RF performance by applying a jet-impingement-based package to MMIC devices. Lian et al. [2] implemented a direct cooling approach by integrating a silicon-based manifold microchannel structure onto a conventional GaN-on-SiC device, showing improvements in thermal management. Nevertheless, comprehensive studies that simultaneously validate both the thermal and RF power amplification performance, while pushing the device to its electrical performance limits, remain scarce.

In this study, we conducted simulations to evaluate the thermal performance enhancement of RF GaN HEMT devices by applying a manifold microchannel direct cooling structure. Furthermore, we fabricated a manifold microchannel structure integrated with a porous metal insert on an actual RF GaN HEMT power amplifier to confirm its manufacturability.

II. METHODOLOGY

a. CFD model setup

Before experimentally evaluating the thermal and hydraulic performance of the RF GaN HEMT with embedded manifold microchannel cooling, a three-dimensional conjugate simulation conducted to provide an effective means estimating these characteristics. The computational analysis utilized ANSYS Fluent v19.2, a widely used solver known for its precision in thermo-fluidic analysis. The microchannel width was set to 30 µm, 50 µm, 100 µm, and 200 µm, while other parameters were set constant. Specifically: Fin width (W_{fin}): 50 µm, SiC thickness (t_{SiC}): 100 µm, Channel height (H_{ch}): 100 µm, Channel length (L_{ch}): 1000 µm, Manifold width (W_{mani}): 300 µm, Manifold height (H_{mani}): 1000 µm. The boundary conditions are mass flow inlet, gate heatflux, and pressure outlet. The inlet mass flow rate is set between 10 ml/min and 80 ml/min, with an inlet temperature of 24°C, and pressure outlet is 0 kPa. A heat flux of 1 MW/cm^2 is applied to the gate area (40 ea × 1 µm × 120 µm). The mass flow rate was selected to not exceed 100 kPa to prevent leaks caused by excessive bonding pressure. Schematic diagram and boundary condition is at Figure 1.

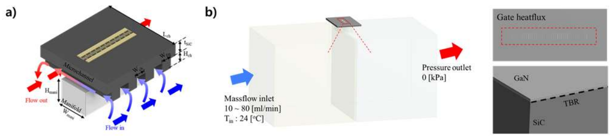

Figure 1. a) Schematic diagram of thermo-fluidic simulation. b) boundary conditinos used in simulation.

b. Fabrication

GaN HEMT devices were fabricated using commercial epitaxial wafers from Cree. Ti/Al/Ni/Au metal stacks were deposited and subjected to rapid thermal annealing at 780 ° C for 40 seconds to form ohmic contacts for the source and drain. The active area was passivated with SiN, and device isolation was achieved through P-dose ion implantation. The damaged SiN layer was removed using buffered oxide etchant (BOE), followed by the deposition of a new 65 nm SiN layer using PECVD. Electrical access to the source and drain was established by RIE etching and deposition of the first metal pad. Subsequently, the SiN layer in the gate region was removed, and a T-gate structure was formed by depositing Ni/Au (40/60 nm). An additional 80 nm SiN layer was deposited for final passivation, and the SiN above the pad area was removed to enable electrical connection. An air-bridge structure was fabricated by Au electroplating.

During backside processing, the device side was protected by bonding to a bare SiC substrate. For the backside process, base metals of Ti/Au 5/8 nm were deposited for Ni electroplating, and a microchannel pattern was defined using photolithography. Ni was electroplated and used as a hard mask, followed by ICP etching with SF_6 gas to form the desired structure. After etching, the Ni and base metal layers were removed, and etching residues were cleaned using HCl-dipped sonication. Fabricated power amplifier is at Figure 2a.

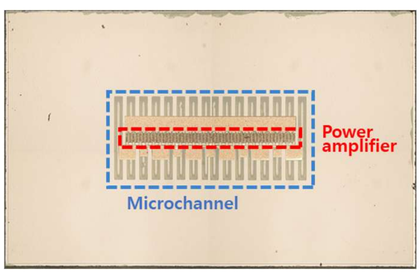

Figure 2. Fabricated AlGaN/GaN HEMT power amplifier with microchannels.

III. Results and discussions

Figure 3a presents the thermal performance analysis results for various microchannel geometries under different flow rates. The device's maximum junction temperature decreases with pumping power, and smaller channel widths (W_{ch}) consistently provide superior thermal performance at the same pumping power. This improvement can be attributed to two factors of in single-phase flow cooling, the available heat transfer area increases with decreasing channel width, and the higher fluid velocity enhances convective heat transfer in the vicinity of the heat source. Figure 3b supports this interpretation by showing the velocity contours at maximum pumping power. For W_{ch}=30 µm, the maximum velocity reaches 16.3 m/s, which is significantly higher than the 12.4 m/s observed for W_{ch}=200 µm. The increased velocity intensifies fluid impingement on the hotspot region, thereby reducing thermal resistance and improving overall device cooling.

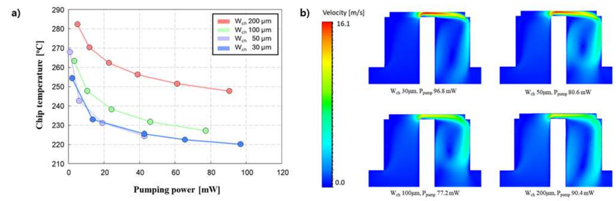

Figure 3. a) Chip temperature versus pumping power for varying channel widths from thermal simulation. b) Fluid velocity contours for different channel widths at maximum pumping power.

A copper inverse opal(CuIO) is adopted as the porous metal structure. This material has previously been utilized in thermal performance experiments using microheaters as a means to enhance heat transfer.[3] To deposit the base metal layer across the backside microchannel of the device for subsequent electroplating, 20/100 nm of Ti/Au was sputtered. A 5 µm polystyrene sphere suspension was then applied by drop casting, followed by sintering in a vacuum oven at 100 °C for 80 minutes to promote neck formation between spheres. The sintered PS template was subsequently filled by electrodepositing copper using an electrolyte solution of 0.5 M $CuSO_4$ and 0.2 M H_2SO_4. After electrodeposition, the PS template was removed by immersing the sample in tetrahydrofuran for more than 24 hours.

As a result of the fabrication process, a CuIO with a thickness of 15 µm was produced by electroplating copper onto a three-layer assembly of 5 µm PS particles, as shown in the SEM image of the CuIO in Figure 4a. The magnified SEM image in Figure 4b reveals that the pore sizes range from 3.8 to 5.4 µm, with an average size of approximately 4.2 µm, while the neck sizes vary between 0.8 and 1.4 µm, yielding a characteristic dimension of about 1 µm.

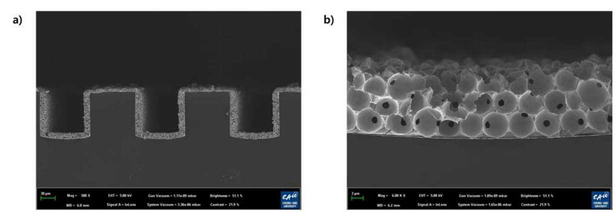

Figure 4. SEM image of CuIO fabricated in a microchannel with W_{ch}=100 µm and W_{fin}=100 µm..

Acknowledgment

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