

A 2.4 GHz RF-DC Rectifier Based on Time-Reversal Duality for Energy Harvesting Applications

Dongjun Joo

*School of Electronic Engineering
Soongsil University
Seoul 06978, Republic of Korea
dongjun3300@soongsil.ac.kr*

Jinho Yoo

*Dept. of Intelligent Semiconductor
Soongsil University
Seoul 06978, Republic of Korea
dbwlsgh@soongsil.ac.kr*

Changkun Park

*Dept. of Intelligent Semiconductor
Soongsil University
Seoul 06978, Republic of Korea
pck77@ssu.ac.kr*

Abstract— In this paper, we designed a 2.4 GHz RF-DC rectifier based on the class-F power amplifier utilizing time-reversal duality. It achieves superior DC power output and high drain efficiency by utilizing a GaN HEMT power amplifier, overcoming the inherent breakdown voltage limits associated with high-power applications. Consequently, it achieved a conversion efficiency exceeding 70% in the input power range of 32-40 dBm. Furthermore, it delivered a maximum DC power output of 7.1 W. Also, it achieved over 60% conversion efficiency across a variable load resistance range of 60-120 Ω .

Keywords— *Class-F power amplifier, RF-DC rectifier, time-reversal duality, wireless power transfer (WPT)*

I. INTRODUCTION

Recently, energy harvesting for autonomous operation of sensor networks and wireless charging for unmanned aerial vehicles (UAV) and electric vehicles (EV) have gained prominence as core infrastructure for the 4th Industrial Revolution [1], [2]. These technologies are essential for overcoming the physical limitations of batteries, reducing maintenance costs, and ultimately establishing a sustainable energy ecosystem. Therefore, wireless power transfer (WPT), enabling medium- to long-range high-power transmission, is gaining prominence in the microwave field. Most circuits currently in use (including both analog and digital) are designed based on transistors, ranging from tens to billions in number. These transistors are active devices requiring DC biasing. This biasing is typically achieved either by converting external AC power into DC using a Schottky diode-based rectifier or by utilizing an internal battery that provides DC power directly [2]. However, the low power efficiency and limitations in output control make conventional rectifiers difficult to apply in WPT systems [3]. Therefore, to implement a WPT system, a high-efficiency, high-power rectifier that converts the RF signal supplied through the receiver (Rx) antenna into DC power usable by edge devices is essential [1].

In this paper, we propose a 2.4-GHz RF-DC rectifier for wireless power transfer that applies the principle of time-reversal duality [4], [5], [6]. The issue of maintaining high efficiency is particularly challenging in conventional Schottky diode-based rectifiers due to their inherent breakdown voltage limit, especially under high power conditions [7]. Unlike conventional rectifiers, this structure leverages a high-efficiency Class-F power amplifier to not only overcome these power limitations but also achieve high efficiency across a wide range of operating frequencies [8]. Furthermore, unlike conventional rectifiers where the output DC voltage is determined by the load resistance, this rectifier can control the DC voltage by adjusting the input power for a fixed load resistance [9]. Therefore, the time-reversal duality, which serves as the basic theory of RF-DC rectification, is described

in Section II. Furthermore, the class-F power amplifier topology, specifically designed for application in the rectifier, and the assist circuit required to realize it, are crucial and are detailed in Section III and Section IV, respectively. Finally, the 2.4 GHz RF-DC rectifier is described in Section V.

II. THEORETICAL ANALYSIS

According to the principle of the time-reversal duality [4], the input and output of a transistor operating as an active switch can be reversed to make it behave similarly to a passive element like a diode. In other words, by reversing the input-output configuration of the conventional power amplifier drive method—DC biasing voltage (V_{GG} , V_{DD}) with gate RF input-drain RF output—and utilizing a structure with DC biasing voltage (V_{GG}) and gate RF input and drain RF input, a new DC voltage is applied to the load resistor (R_{load}). Therefore, as shown in Fig. 1, a self-synchronous rectifier can be created from the power amplifier. For this operation, the assist circuit must apply signals with appropriate amplitude and phase to each port of the power amplifier to achieve positive voltage rectification and high efficiency.

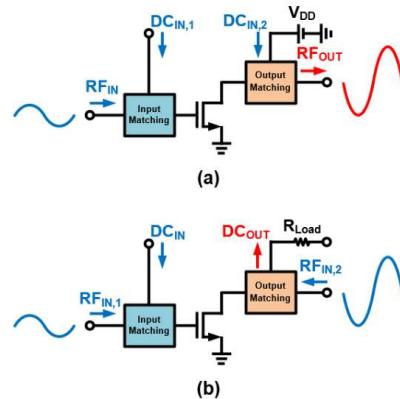


Fig. 1. Power flow of the RF-DC rectifier using time-reversal duality: (a) power flow of the conventional PA and (b) power flow of the rectifier applied time-reversal duality.

A class-F power amplifier is a highly efficient amplifier that minimizes power loss by configuring a matching network to ensure the transistor's drain voltage follows a square waveform and the drain current follows a half-sine waveform, thereby preventing simultaneous conduction between the waveforms [8]. This is theoretically achieved through harmonic control at the drain, where the impedance for odd-order harmonics of the fundamental frequency is controlled to be open, and the impedance for even-order harmonics is controlled to be short [5]. The power amplifier used in this paper requires not only load-pull matching for optimal amplification but also impedance matching considering the

assist circuits connected to both ends of the power amplifier. Since this rectifier is applicable to any arbitrary application, this paper performed impedance matching to bring the power amplifier and assist circuits as close as possible to 50Ω . Particularly, since load-pull matching is variable depending on the input impedance of the input port connected to the gate, the design paid careful attention to the impedance matching between the phase-shifting line of the interconnected assist circuit and the input port.

III. POWER AMPLIFIER DESIGN

Fig. 2 shows the proposed class-F power amplifier (PA). Harmonic control in the microstrip line is achieved by adjusting the signal line length using the input impedance (Z_{in}) formula from the lossless transmission line (TL) in (1). Specifically, as shown in (2), when the load impedance (Z_L) of the matching line is in a special state (open or short), Z_{in} at the point corresponding to a quarter-wavelength from the load appears as the inverted form of Z_L .

$$Z_{in}(l) = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \quad (1)$$

$$Z_{in,open}\left(\frac{\lambda}{4}\right) = Z_0 \frac{1}{j \tan\left(\frac{2\pi\lambda}{\lambda} \frac{1}{4}\right)} = 0 \quad (2)$$

This can be applied to limit the drain impedance to open or short at specific frequencies. The harmonic control discussed in this article was applied up to the 3rd harmonic. The 3rd harmonic is utilized with the fundamental frequency to shape the drain voltage, whereas the 2nd harmonic is grouped with other even harmonics (which are ideally shorted) and is independent of the odd harmonics. For example, in the case of an open-circuited TL (OCTL), $Z_{in}\left(\frac{\lambda}{4}\right)$ behaves like an inverting short-circuited TL (SCTL) for the fundamental frequency and the 3rd harmonic, but it remains identical to OCTL for the 2nd harmonic [8].

The drain of the PA used in this paper is connected simultaneously to both the RF input and DC output of the RF-DC rectifier. In other words, the amplified signal formed at the drain can act as ripple on the DC output. Therefore, the proposed DC matching network is designed to have a high input impedance at the drain—appearing as a nearby open circuit—for both the fundamental frequency and its harmonics, and a series resistor is used at the gate for stability.

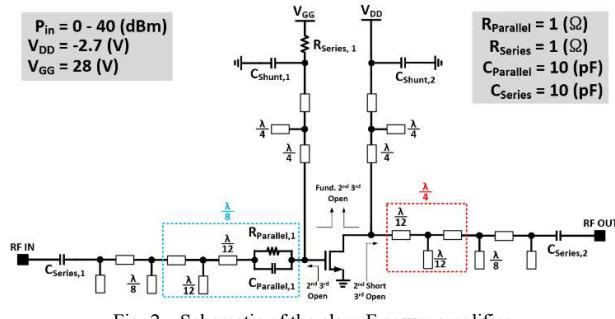


Fig. 2. Schematic of the class-F power amplifier.

A. DC Matching Network (DCMN)

Fig. 3 shows that the DC Matching Network (DCMN) with a $\lambda/4$ -TL makes the fundamental and 3rd harmonic impedances appear open. The 2nd harmonic impedance can

be controlled using TL_1 , while the fundamental and 3rd harmonic impedances remain unaffected by changes in TL_1 's length. Therefore, tuning TL_1 ensures all frequencies (fundamental, 2nd, 3rd) in the DCMN are high impedance nearby open.

B. Output Matching Network (OMN)

At the drain, the DCMN fundamental, 2nd, and 3rd impedances all appear open. Therefore, the 2nd harmonics of the OMN connected to Port-2 are controlled to be short, and the 3rd harmonics are controlled to be open [6]. Furthermore, (3) shows that the input impedance (Z_{in}) at the point corresponding to half-wavelength is equal to the load impedance (Z_L). Therefore, in our proposed OMN, TL_2 is tuned near $\lambda/6$ to control the 2nd harmonics to be short. TL_3 and TL_4 are used for load-pull matching.

$$Z_{in}\left(\frac{\lambda}{2}\right) = Z_L \quad (3)$$

C. Input Matching Network (IMN)

Low-frequency oscillation is caused by a feedback loop formed due to finite impedance at AC ground, where a very small signal is amplified through the feedback loop, leading to oscillation. Inserting a series resistor is one effective method to improve stability. As shown in Fig. 1, a DC voltage is applied to the load resistor via the OMN, outputting rectified power. Therefore, the series resistor in the OMN of the power amplifier not only acts as additional resistance to the load resistance R_{Load} but also changes the power gain or PAE. Conversely, inserting the series resistor in the gate DC biasing, along with the parallel RC connected to the gate, does not significantly affect the load resistance (R_{Load}) or the output matching network (OMN), unlike the resistor placed in the OMN. At this point, high resistance inhibits amplification, so a small resistance of 1Ω is used in this paper.

Therefore, as before, since the DCMN fundamental, 2nd, and 3rd impedances are all open, control the 2nd and 3rd harmonics of the IMN connected to Port-1 to satisfy the ideal class-F PA condition. For $\lambda/8$, TL_5 is tuned near $\lambda/24$, while TL_6 and TL_7 are used for load-pull matching.

D. Simulated Results

Fig. 3 shows the EM-simulated load-pull and harmonic control results, including the contours of power added efficiency (PAE) and output power (P_{out}) at the drain. The PAE contour is shown as dashed lines at 2% intervals within the range of 63.6% to 69.6%, while the output power contour is shown as solid lines at 0.5 dBm intervals within the range of 40.6 dBm to 42.1 dBm.

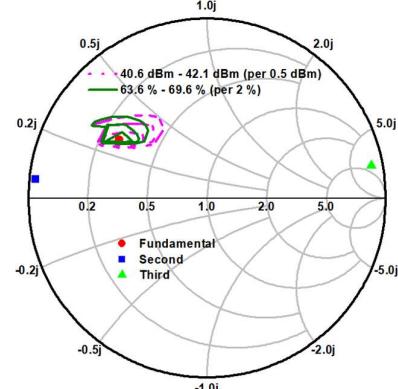


Fig. 3. Simulated results of the load-pull and harmonic controls.

Consequently, the fundamental impedance was load-pull matched at the point where both PAE and P_{out} were maximized. Since the 2nd harmonic satisfied the short condition and the 3rd harmonic satisfied the open condition, it was confirmed that the device operates as intended as a class-F power amplifier.

Fig. 4 shows the power gain and drain efficiency of the Class-F power amplifier at 2.4 GHz as the input power (P_{in}) is swept from 0 dBm to 40 dBm. Consequently, the drain efficiency exceeds 80% starting at 28 dBm, with a maximum drain efficiency of 87%. Fig. 5 shows that power saturation occurs at P_{in} is 28 dBm, which is related to the coupler in the assist circuit. This will be explained in the next section.

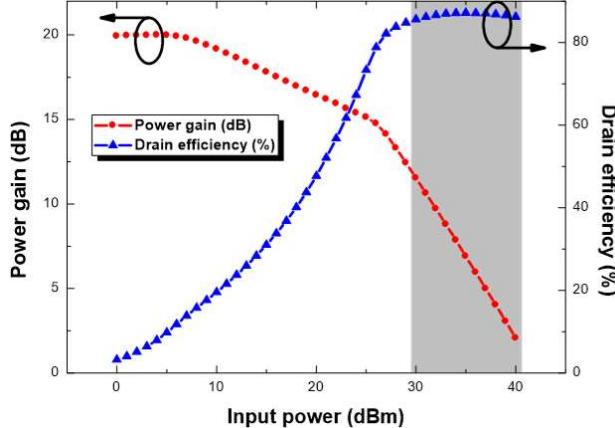


Fig. 4. Simulated power gain and drain efficiency of the class-F power amplifier at 2.4 GHz.

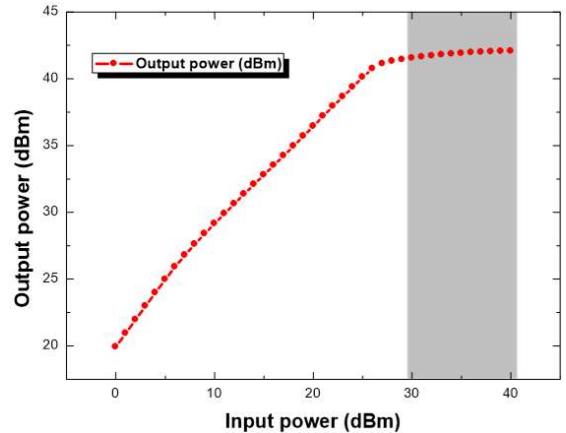


Fig. 5. Simulated output power of the class-F power amplifier at 2.4 GHz.

IV. ASSIST CIRCUIT DESIGN

To satisfy the principle of time-reversal duality [4], the signal at the gain point must be applied to the gate with an appropriate phase difference [5], [9]. Theoretically, the power gain in Fig. 4 does not satisfy flat gain (e.g., P_{in} is 28 dBm), so the assist circuit is configured using a coupler corresponding to the power gain at the onset of power saturation (13 dB in this case). However, losses occur as the signal passes through the IMN and OMN, necessitating adjustment of the optimal coupling ratio for operation. Experimental results confirmed that a 10 dB coupler [10] is suitable for this structure.

The phase shifting line delays the phase of the signal output from port-3 of the coupler. This ensures the signal applied to the gate has an approximate 180° phase difference with the signal from port-2 of the coupler, thereby outputting a positive DC voltage to the load resistance with maximum efficiency. Therefore, the assist circuit described in this paper consists of a 10 dB coupler and a phase shifting line. For stable operation and connection, the rectifier's RF input port was impedance matched precisely to 50Ω . Conversely, the power amplifier's input/output ports were matched such that the real part was near 50Ω , with the input port reactance minimized (near zero) and the output port reactance having a positive value (inductive).

V. RF-DC RECTIFIER DESIGN

A. Topology of the RF-DC rectifier

Fig. 6 and Fig. 7 show the overall schematic and layout reflecting the EM simulation results of the RF-DC rectifier operating at 2.4 GHz. Series capacitors for DC blocking and parallel C and parallel R networks for low-frequency stability were implemented using lumped elements. Additionally, the series resistor in the gate bias (V_{GG}) improved stability at low frequencies. The overall module size is approximately $70\text{mm} \times 70\text{ mm}$.

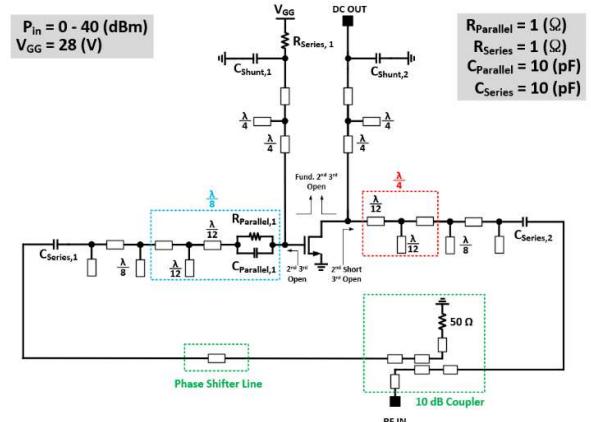


Fig. 6. Schematic of RF-DC rectifier based on class-F power amplifier.

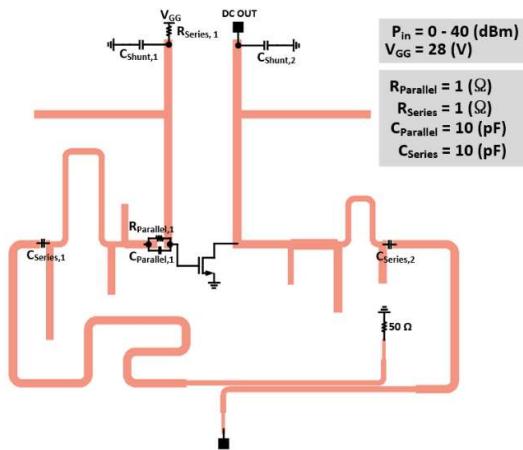


Fig. 7. Layout of RF-DC rectifier based on class-F power amplifier.

B. Simulated Results

Fig. 8 shows that our proposed power amplifier satisfies over 70% RF to DC conversion efficiency starting from the gain saturation onset point P_{in} is 28 dBm, with a maximum conversion efficiency of 72%. This conversion efficiency demonstrates a superior result compared to other works [3], [6]. The output DC power increases exponentially from this point, achieving the maximum output DC power of 7.2 W at P_{in} is 40 dBm. Fig. 1 shows that a series load resistance (R_{Load}) exists at the rectifier's DC output port, generating a DC voltage. Fig. 9 shows the RF-to-DC conversion efficiency for this variable R_{Load} at P_{in} is 35 dBm. Consequently, the RF-DC rectifier demonstrates a stable conversion efficiency exceeding 60% for R_{Load} values ranging from 60 to 120 Ω .

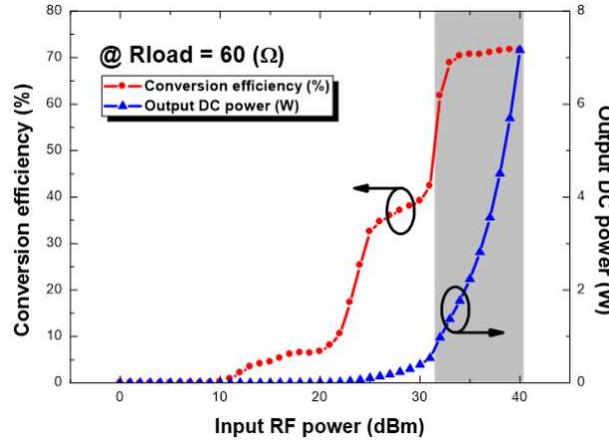


Fig. 8. Conversion efficiency and Output DC power of the RF-DC rectifier.

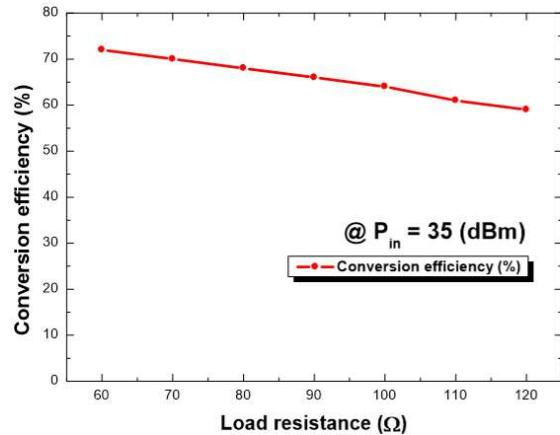


Fig. 9. Conversion efficiency of the RF-DC rectifier with varying load resistance.

VI. CONCLUSION

A 2.4 GHz class-F RF-DC rectifier was designed based on time-reversal duality. This utilizes a GaN HEMT, resulting in the design of the class-F power amplifier with a maximum drain efficiency of 87%. This power amplifier exhibits power saturation at P_{in} exceeding 28 dBm, with the output power converging to 42 dBm at this point. For high-efficiency conversion of the RF input signal to a DC output signal via time-reversal duality, it is essential that signals with appropriate magnitude and phase difference are applied to the

power amplifier's input and output. Therefore, the proposed RF-DC rectifier consists of the power amplifier, a phase-shifting line, and a 10 dB coupler. In conclusion, the maximum conversion efficiency of the RF-DC rectifier is 72% when R_{Load} is 60 Ω , and it achieves over 70% conversion efficiency in the range where P_{in} is 28 dBm or higher. It demonstrates comparable performance to other works [3], [6]. Furthermore, it maintains over 60% conversion efficiency even when R_{Load} varies between 60 and 120 Ω .

Unlike conventional Schottky diode-based rectifiers, this RF-DC rectifier has significantly higher breakdown voltage limits, especially under high-power conditions [7]. This characteristic enables highly efficient energy harvesting in high-input power environments. Furthermore, leveraging the GaN HEMT offers benefits beyond high-power operation: unlike conventional rectifiers that typically support only up to several tens of GHz, this structure can rectify higher frequency signals. Considering that the chip size is proportional to the operating wavelength, this architecture also suggests a potential advantage in size reduction through integration.

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