A 2-Stage Differential FD-SOI Low-Noise Amplifier for 6G Front-End Applications

Geunwoo Park
School of Electronic Engineering
Soongsil University
Seoul 06978, Republic of Korea
geonwoo4608@soongsil.ac.kr

Chaeyoon Kim
Dept. of Intelligent Semiconductors
Soongsil University
Seoul 06978, Republic of Korea
kcy01@soongsil.ac.kr

Changkun Park
Dept. of Intelligent Semiconductors
Soongsil University
Seoul 06978, Republic of Korea
pck77@ssu.ac.kr

A. Introduction

Recently, the demand for 6G communication systems has significantly increased, leading to rapid research and development of such technologies. In this paper, the low-Noise Amplifier (LNA) plays a crucial role in the receiver front-end module. Positioned at the input stage of the system, the LNA greatly impacts the overall sensitivity and noise performance of the communication link. In 6G communication, the LNA must provide sufficient gain while maintaining a low noise figure (NF) and ensuring stability over a wide frequency range. To meet these requirements, a 2-stage LNA structure based on FD-SOI technology was employed to achieve the target specification.

B. Low noise amplifier design

Figure. 1 shows the designed 2-stage differential LNA [1]. The first stage is implemented as a low-noise amplification stage, focusing on minimizing the NF through source degeneration and careful impedance matching. This stage ensures that the overall receiver sensitivity is preserved. The second stage is designed as a differential gain stage to provide sufficient amplification while maintaining linearity and driving capability for subsequent circuits. To further enhance the stability of the proposed LNA, a neutralizing capacitor is applied in the differential stage, where it offsets the parasitic capacitance of the transistors, thereby improving bandwidth and overall circuit performance [2]. In addition, the parallel capacitors and transformers are optimized through simulation to ensure impedance matching and stable wideband operation. Through these design choices, the proposed LNA achieves low noise figure, sufficient gain, and robust stability, making it well suited for 6G FD-SOI front-end applications [3].

C. Design results

Figure. 2 presents the S-parameters of the designed LNA, while Fig. 3 shows the simulated NF. From the S-parameters in Fig. 2, it is evident that proper input and output matching has been achieved, with both S_{11} and S_{22} maintained below –10 dB across the 7–9 GHz. In addition, the forward gain S_{21} exceeds 20 dB throughout the same band, confirming sufficient amplification. Figure. 3 demonstrates that the proposed LNA achieves a NF lower than 2 dB across 7–9 GHz, validating its low-noise performance and suitability for 6G FD-SOI front-end module applications.

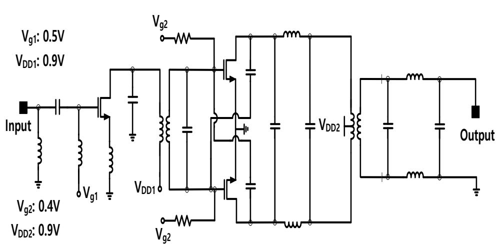

Fig. 1. Schematic of 2Stage LNA

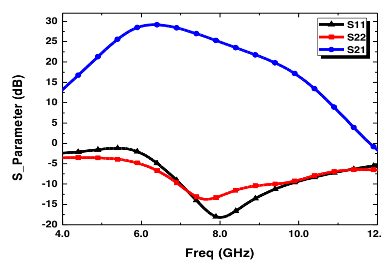

Fig. 2. Results of Simulation S-parameter

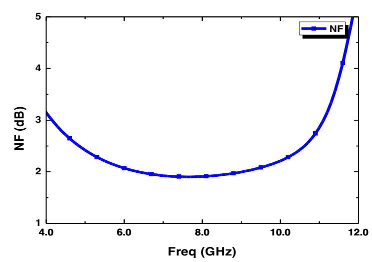

Fig. 3. Results of Simulation Noise Figure

ACKNOWLEDGMENT

This work was supported by the Institute of Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (Ministry of Science and ICT, MSIT) under Grant RS-2024-00398318.

REFERENCES

[1] X. Fan, H. Zhang and E. Sánchez-Sinencio, "A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA," IEEE Journal of Solid-State Circuits, vol. 43, no. 3, pp. 588–597, Mar.

[2] J.-E. Lee and C.-Y. Kim, "Design of 1:1 transformer-based 2-stage differential low-noise amplifier for W-band radar," IDEC Journal of Integrated Circuits and Systems, vol. 10, no. 2, pp. –, Apr.

[3] M. Rack, S. Wane, D. Bajon, J.-P. Raskin, and D. Lederer, "Low Power K- and Ka- Wideband LNA Design in 22 nm FD-SOI Using Transformer-Tuned Input," Proc. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pp. 1–3, 2025.

[4] C. Kim, H. Yoon, J. Lee and C. Park, "Ka-Band Two-Stage Low-Noise Amplifier with Low-Q Inductor Technique Using 28-nm FD-SOI single CMOS Process for Beamforming Systems," *2025 5th International Conference on Electronics, Circuits and Information Engineering (ECIE)*, Guangzhou, China, 2025, pp. 540-543