UART Error Detection Using Cyclic Redundancy Check

Hongmin Jung
School of Electronic Engineering
Soongsil University
Seoul, Republic of Korea
jhm9145@soongsil.ac.kr

Seongsoo Lee
School of Electronic Engineering, Department of Intelligent Semiconductor
Soongsil University
Seoul, Republic of Korea
sslee@ssu.ac.kr

Conventional UART offers only minimal error detection via optional parity and stop bits. We propose a lightweight byte-aligned framing layer atop UART that adds explicit Length and Sequence fields for loss/duplication detection and appends an 8-bit cyclic redundancy check (CRC-8/ATM, polynomial 0x07). The hardware architecture remains compact—comprising a Tick Generator that derives the UART bit time from the system clock, an APB-mapped register block for control and status, and paired transmit/receive paths with CRC generation/verification—while the firmware interacts through an interrupt interface (TX_DONE, RX_DONE, crc_error) that enables frame-level I/O and optional retransmission upon CRC failure. This scheme achieves rapid resynchronization after disturbances and substantially improves reliability without sacrificing UART simplicity or FIFO-peripheral compatibility.

A. Architecture and module

In the proposed architecture, a Tick Generator derives the UART bit-time from the system clock, and a lightweight Register Block (APB) exposes control/status . The TX and RX modules send and receive framed data, respectively. CRC operation uses an 8-stage LFSR (CRC-8/ATM, poly 0x07). CRC_gen computes and appends the check byte on transmit. CRC_check recomputes it over the same region and flags a mismatch as crc_error on receive.

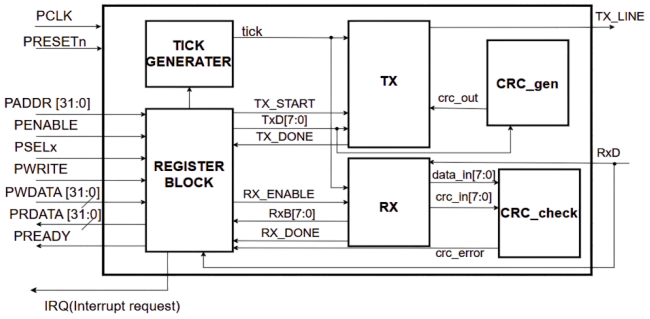

Fig. 1. Architecture and module

B. CRC-8

The design uses CRC-8/ATM with generator polynomial $G(x)=x^8+x^2+x+1$ (poly 0x07), transmitter and receiver must employ identical parameters. Implemented as an 8-stage LFSR, each input bit (processed MSB-to-LSB) forms a feedback bit as the XOR of the CRC's current MSB and the data bit; the register shifts left by one, and, when the feedback is 1, it is XORed with 0x07; after all bytes are consumed, the final CRC (with xorout 0x00) is emitted as the check byte.

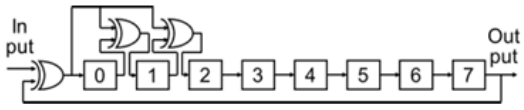

Fig. 2. Architecture of CRC hardware

ACKNOWLEDGMENT

THE AUTHORS THANK PROF. SEONGSOO LEE FOR HIS GUIDANCE AND VALUABLE DISCUSSIONS REFERENCES. THIS WORK WAS SUPPORTED BY KOREA EVALUATION INSTITUTE OF INDUSTRIAL TECHNOLOGY (KEIT) FUNDED BY THE KOREA GOVERNMENT (MOTIE). (RS-2022-00154973)

REFERENCES

[1] Y.-H. Seo and D.-w. Kim, “UART-to-APB Interface Circuit Design for Testing a Chip,” Journal of Advanced Navigation Technology (JANT), vol. 21, no. 4, pp. 386–393, Aug. 2017

[2] Koopman, P.; Chakravarty, T. “Cyclic Redundancy Code (CRC) Polynomial Selection for Embedded Networks,” *Proceedings of DSN 2004*, pp. 145–154