Experimental Study on Optimized Operating Conditions of 4T2C eDRAM Compute in Memory

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A. Introduction and Motivation

This paper extends the existing logic-compatible eDRAM-based Compute-in-Memory (CIM) architecture by providing a refined analysis of operational characteristics using the same 4T2C ternary eDRAM cell. Unlike prior studies that emphasized retention time enhancement with MOM capacitors, embedded ADC design, and performance evaluation on MNIST/CIFAR-10, this work focuses on experimental optimization under a supply voltage of 5 V. An automatic linear-region search procedure, implemented in code and applied to NMOS I–V characteristics, was used to identify the device's linear operating range (Fig. 1(a)). In addition, precharge voltage and cell capacitance were optimized to evaluate the linearity and stability of voltage-based multiply-and-accumulate (MAC) operations.

B. Architecture

The proposed architecture employs a voltage-accumulation scheme in which bitline voltage drop directly represents the MAC results, thereby ensuring a rail-to-rail dynamic range. Separation of read and write bitlines prevents write disturbance, while the 4T2C cell structure enables ternary weight storage of −1, 0, and +1.

C. Experimental Methodology and Results

Through simulation (Fig. 1(c)), it was confirmed that the optimal operating conditions are achieved with a weight voltage of 0.8 V, precharge voltage of 3.2 V, cell capacitance of 20 fF, and an operating range of 2.0–3.2 V, as shown in Fig. 1(b). For a 128-cell array, the system achieved an average voltage drop of 0.855 mV, a standard deviation of 0.0275 mV, and a correlation coefficient of 0.99885, demonstrating high linearity and uniformity."

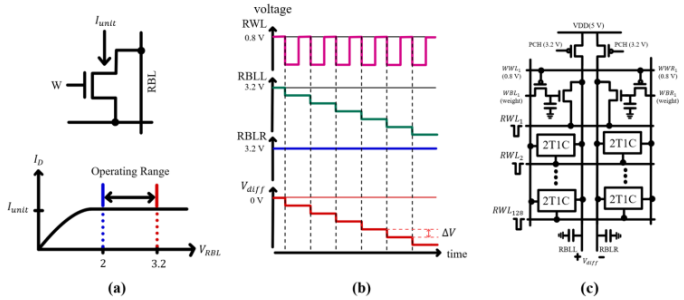

Fig. 1. (a) Dot product operation in a column of eDRAM array (b) Simulation output for WL set High and WR set Low (c) Proposed experimental setup based on the conventional 4T2C eDRAM Compute-in-Memory array

D. Conclusion

Therefore, the proposed architecture is expected to make a significant contribution to energy-efficient and high performance in-memory computing for mobile edge devices.

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REFERENCES

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