A GaN HEMT-Based Class-F Rectifier for Wireless Energy Harvesting at 2.4 GHz

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***Abstract*— The accelerating shift towards renewable energy utilization and transition at the corporate and national levels, driven by the increasing importance of climate change response and carbon neutrality, highlights the growing need for energy harvesting technologies. This paper proposes a class-F rectifier for power reception in 2.4 GHz wireless power transmission systems. The rectifier is designed based on the principle of time reversal duality, where the output and input ports of a high-efficiency class-F power amplifier (PA) are inverted. The class-F PA achieves high efficiency by optimizing harmonic impedances through the placement of individual tuning circuits for the fundamental, second, and third harmonics within its matching network. The implemented rectifier achieved a DC output power of approximately 7.1 W and a peak RF-to-DC power conversion efficiency (PCE) of about 72.8% under conditions of 40 dBm input power and a 60 Ω DC load. This demonstrates the validity of the proposed high-efficiency design strategy.**

Keywords - Class-F, Energy harvesting, GaN HEMT, Harmonic tuning, Power amplifier, Rectifier, Time reversal duality.

I. Introduction

The escalating importance of climate change mitigation and carbon neutrality is accelerating the mandatory adoption and transition toward renewable energy at the corporate and national levels [1]. While most efforts focus on large-scale energy production, such as wind and solar power, this study focuses on the contrasting aspect of reusing waste energy resulting from system losses, specifically the power dissipated by attenuators [2]. This approach signifies that energy harvesting technology can maximize the overall system efficiency, ultimately reducing initial energy consumption and, consequently, contributing significantly to the realization of carbon neutrality [3].

However, conventional diode-based rectifiers [4] exhibit a sharp degradation in conversion efficiency due to increased switching losses in the high-frequency [5], W-class high-power applications targeted by this study, thereby limiting their practical implementation. To overcome these limitations and improve the constraints of power conversion in high-frequency environments, this study adopts a transistor (TR)-based rectifier structure [6]. Specifically, we utilize the GaN HEMT (High Electron Mobility Transistor), a wide-bandgap (WBG) transistor known for its high breakdown voltage characteristics and superior thermal stability [7], to fundamentally improve the power capacity and efficiency of conventional rectifiers.

The design of this rectifier is achieved by inversely designing a high-efficiency PA, following the principle of time reversal duality [8]. Specifically, by applying the class-F PA topology, which can achieve very high efficiency by controlling the output voltage and current waveforms into ideal forms, the rectifier is designed to achieve high efficiency. Consequently, this paper presents a novel methodology for systematically controlling both the input and output harmonics of the class-F PA [9], successfully designing and validating the performance of a high-efficiency GaN-based class-F rectifier [6].

II. Theoretical Analysis and Design Methodology

A. Time Reversal Duality

Time reversal duality is a principle of circuit theory that interprets the waveform relationship of a signal passing through a specific network by reversing it with respect to the time axis. This principle allows us to derive the waveform relationship between an energy-supplying circuit and an energy-consuming circuit.

According to the principle of time reversal duality, the role of the PA input is exchanged with the rectifier output, and the rectifier input is exchanged with the PA output [10]. Furthermore, the waveforms are reversed with respect to the time axis. This relationship ensures that the high-efficiency condition of the PA is transformed and maintained as the minimum-loss operating condition for the rectifier. Therefore, it is possible to design a high-efficiency rectifier by inversely designing the topology of a proven high-efficiency PA, such as the class-F PA [8].

$$v_{PA}(t) = v_{RE}(-t)$$
$$i_{PA}(t) = -i_{RE}(-t)$$

B. Class-F Operation and Conditions

The class-F operation is based on controlling the output harmonic impedances to achieve high efficiency. This mode of operation shapes the V_{DS} waveform by adding odd harmonic components to approximate a square wave, and shapes the output I_{DS} waveform by removing even harmonic components to create a half-sine wave.

Through this waveform engineering, the transistor is maintained with V_{DS} at zero when it is turned on, and I_{DS} at zero when it is turned off in Fig. 1 Consequently, this operation realizes a switching mode where the peak values of V_{DS} and I_{DS} do not overlap simultaneously, theoretically eliminating switching losses and allowing efficiency to approach 100% [11].

However, in practical circuit design, the energy of high-order harmonics (n ≥ 4) sharply decreases, and the complexity of the matching network required to control them

becomes excessively large [12]. Therefore, at a practical level, only the second and third harmonics are primarily considered. Consequently, since the waveform cannot perfectly reach the ideal square wave and half-sine wave, the Class-F PA typically exhibits an efficiency of around 75% to 85% [11]. To overcome these realistic efficiency limitations, precise phase adjustment of the class-F gate and drain is essential [6].

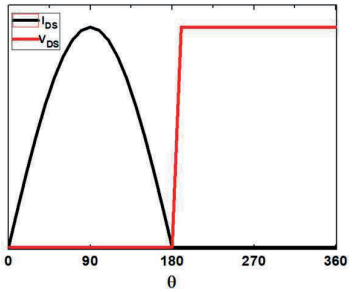

Fig. 1. Ideal drain voltage and current waveforms for class-F

C. Rectifier Operation Based on Time Reversal Duality

The implementation of the rectifier begins with the fundamental principle of time reversal duality, as previously explained. According to this principle, the role of the PA input is exchanged with the rectifier output, and the PA output is exchanged with the rectifier input [10].

At this point, a coupler is necessary to precisely deliver the rectifier RF input signal to the transistor gate and to distribute power to the drain [6]. Furthermore, a phase shifter is added to precisely control the transistor phase relative to the RF input signal, ensuring the achievement of the class-F minimum loss switching condition [8].

III. Circuit Design and Implementation

A. Harmonic Tuning circuit

The design was carried out based on the operating conditions of a class-F PA, which requires a second harmonic short and third harmonic open harmonic structure [11].

As shown in Fig. 2 smith chart, the output matching network was implemented to satisfy these class-F conditions.

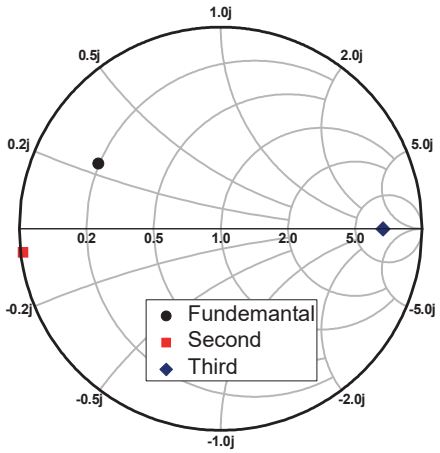

Fig. 2. Output matching network smith chart

As depicted in the PA circuit diagram in Fig. 3, this study implemented harmonic tuning for comprehensive harmonic control.

Both the gate and drain terminals of the transistor were designed to satisfy second and third harmonic open conditions. Additionally, the V_{GG} and V_{DD} bias lines were designed to present fundamental and third harmonic open conditions, completing the overall harmonic control structure.

Consequently, this input and output harmonic tuning design allows for the creation of a high-efficiency class-F PA by controlling the harmonic paths within the matching network while maintaining the class-F mode. Due to time reversal duality, the rectifier can also achieve high-efficiency output [8].

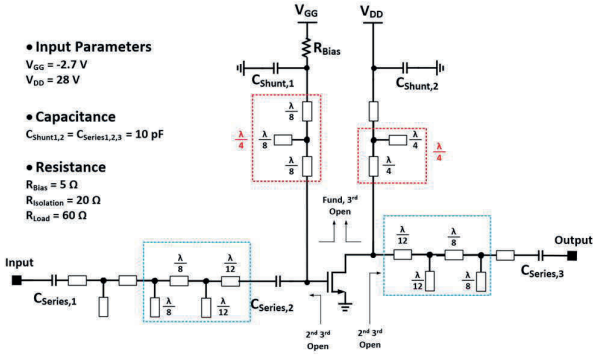

Fig. 3. Class-F power amplifier schematic

B. Coupler and Phase Shifter

Referring to Fig. 4 the coupler was designed to target approximately 14 dB, which is the point where the flat gain of the PA begins to drop sharply. This is intended to satisfy the optimal operating conditions by injecting the PA maximum efficiency driving condition as a signal to the gate of the rectifier, based on the principle of time reversal duality.

The phase shifter was designed with a focus on achieving a 180 ° phase shift to align the phase of the coupled signal with the voltage and current waveforms at the drain. This precise phase alignment is crucial because, shown in Fig. 1, aligning the phase of V and I is essential for establishing the class-F minimum loss switching condition [11], thus requiring precise control.

In the actual circuit implementation, the coupler was designed with a coupling factor of 13 dB, taking into account the insertion loss of the phase shifter. Furthermore, the phase shifter was adjusted according to the phase conditions of the coupler and PA to ensure the high-efficiency class-F minimum loss condition was guaranteed.

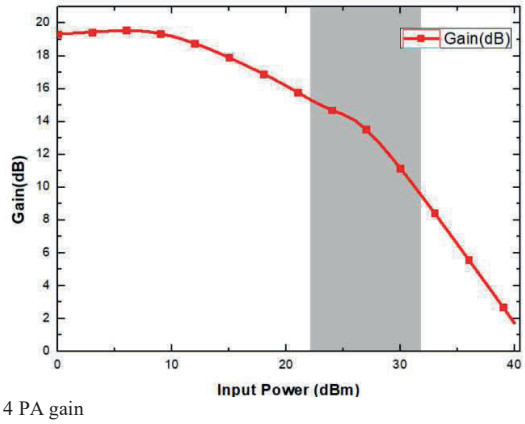

Fig. 4 PA gain

C. Rectifier Configuration

The rectifier operation is implemented by using a coupler to deliver the input signal and a phase shifter to align the phase between the gate and the drain, which is essential for ensuring the minimum-loss switching condition derived from the Class-F principle [11]. By connecting a dc load resistance R_{DC} at the PA V_{DD} terminal, it can be confirmed that the RF power is converted into dc power through this load. Consequently, the rectifier can satisfy both the high-efficiency conditions of the class-F PA and the time reversal duality principle [8].

The schematic-level simulation results showed a maximum PCE of 75.6% at a 2.4 GHz and 40 dBm (10 W) input. This efficiency is significantly higher than that of conventional diode rectifiers in W-class high-power regimes [4], validating the proposed GaN HEMT-based class-F structure. Under this condition, the maximum power applied to the gate was 9.8 W, and the maximum P_{DC} was 7.0 W.

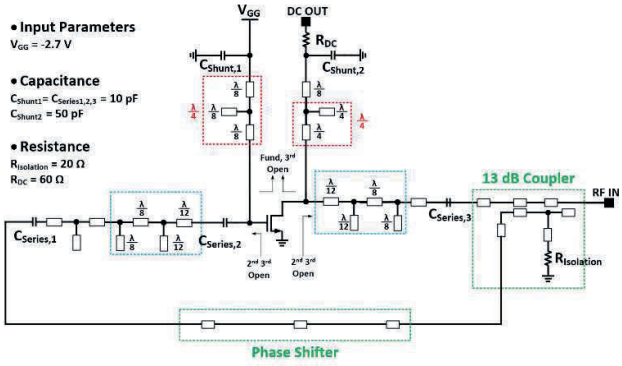

Fig. 5 Rectifier schematic

D. EM Simulation result

The rectifier layout used for the electromagnetic (EM) simulation is presented in Fig. 6, and it was implemented with dimensions of width 52.1 mm Height 70.1 mm. The final simulation results are shown in Fig. 7, revealing a maximum PCE of 72.8% and a dc output power P_{DC} of 7.1 W Other performance metrics are summarized in Table 1.

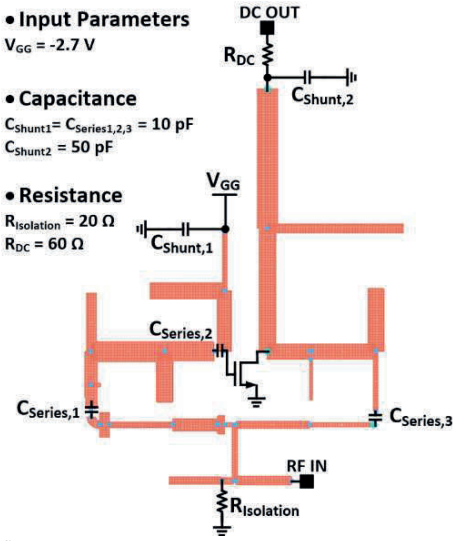

Fig. 6 Rectifier EM

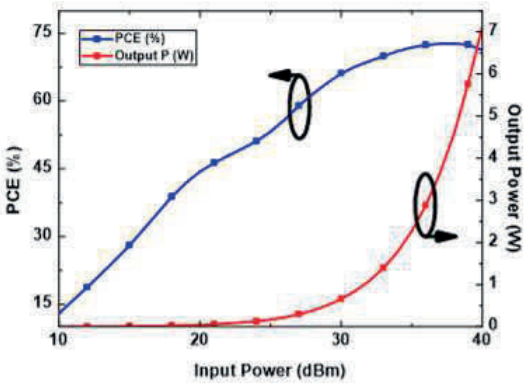

Fig. 7 Rectifier result with EM PCE (%) and P_{DC} (W)

EM simulation results confirmed a PCE drop of 2.8% compared to the schematic-level simulation. Gate P_{IN} is an indicator showing how efficiently the 40 dBm (10W) input power is delivered to the transistor gate after passing through the coupler and phase shifter. During the EM layout tuning process, the gate P_{IN} was successfully improved by optimizing the length of the coupler and phase shifter. This increase in P_{IN} was the main reason for obtaining a higher P_{DC} value than before the EM implementation, which is confirmed by the simultaneous improvement in the output V_{DC} and I_{DC}

TABLE 1 COMPARISON OF OUTPUT METRICS UNDER EM

OUTPUT METRICS		
Parameter	**Schematic**	**EM**
PCE (%)	**75.6**	**72.8**
P_{DC} (W)	**7**	**7.1**
Gate P_{IN} (W)	**9.8**	**9.9**
V_{DC} (V)	**20.5**	**20.7**
I_{DC} (A)	**0.34**	**0.35**

IV. CONCLUSIONS.

A rectifier was implemented at the 2.4 GHz, applying the time reversal duality principle. This structure integrates a class-F power amplifier structure, including a harmonic tuning network with coupler and phase shifter. As a result, it yielded a maximum PCE of 72.8% and P_{DC} of 7.1 W. This performance validates its sufficient usability for harvesting purposes in watt level wireless power reception applications.

Currently the implementation is at the PCB level which presents limitations due tSo its large size. Furthermore, by targeting only the 2.4 GHz single-frequency, its application range is restricted. Future research is planned to focus on size reduction through IC level integration design and expansion to higher frequency bands for utilization in various applications.

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