28GHz 6-Bit QAF based Active Phase Shifter

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In this paper, a 28 GHz 6-bit active type phase shifter for phased array beamforming application is proposed. The input signal is converted into a differential signal by the input transformer, and the differential signal is converted into an I/Q signal by the quadrature all pass filter. According to the input bit, the Current DAC can change the phase by adjusting the current ratio of the I/Q signal, and can cover 360° with a resolution of 5.625°. Implemented in 65 nm CMOS technology, the proposed phase shifter achieves measured RMS phase error of 2.8°-3.3° and RMS gain error of 0.9 dB – 1.1 dB and P1dB of 3.2 dB over 26.5 GHz to 29.5 GHz.

Keywords—phase shifter, quadrature all pass filter (QAF), millimeter wave

I. INTRODUCTION

With the advancement of the CMOS process, the line width has been reduced to the nanometer scale, allowing more circuits to be integrated on a single wafer, and the minimum gate length has been reduced, making it possible to design high speed circuits. And the supply voltage is also reduced accordingly, so the power consumed by the circuit is also reduced.

However, it is difficult to design an RF circuit because the performance such as gain and output power of the internal components of the RF chain is deteriorated due to the decrease of the supply voltage according to the development of the CMOS process. In addition, as the operating frequency of the circuit approaches the millimeter wave band, the output

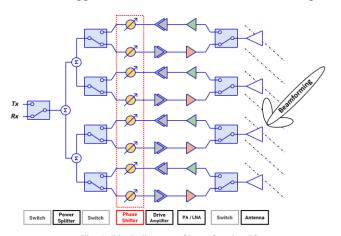


Fig. 1 Block diagram of beamforming IC

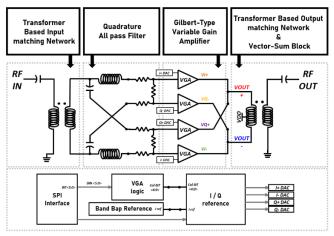


Fig. 2 Block diagram of phase shifter

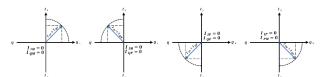


Fig. 3 Phase according to the sum of the I/Q vectors

power of the power amplifier (PA) is required to be higher due to the larger propagation path loss. But designing a PA that satisfies such performance is difficult due to the trade-off described above. Therefore, instead of using a single RF chain to transmit signals in all directions, the beam must be shaped to send a strong signal in the desired direction by exciting signals of different phases into each array antenna. To do this, a beamforming IC (BFIC) as shown in Fig. 1. is needed.

The structure of each channel of the BFIC is determined by whether the phase shifter is active, passive, unidirectional, or bidirectional. For this reason, the phase shifter is a key component of the beamforming technology. In this paper, an active QAF-based vector sum phase shifter is proposed.

II. DESIGN OF THE PROPOSED PHASE SHIFTER

The block diagram of the proposed vector sum phase shifter is composed of input transformer (TF), QAF, four VGAs, output TF, and DAC to control each VGA as shown in

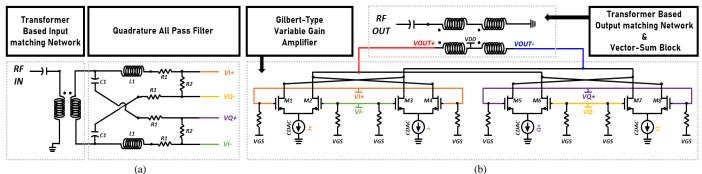


Fig. 4 Schematic of phase shifter (a) input transformer and QAF (b) gilbert type analog adder

Fig. 2. When the RF signal passes through the input TF, it is converted to a differential signal, and this signal passes through the QAF and is divided into a quadrature signal with a phase difference of 90 °, and each converted Quadrature signal is applied to the input of four VGAs. As shown in Fig. 3. To change the phase, the sign and magnitude of the IQ vector must be adjusted and summed. According to the input bit, the DAC adjusts the gain of each VGA and the output TF adds these vectors to shift the phase.

As shown in Fig 4, TF converts the input signal into a differential signal or sums the I and Q vector signals of the VGA. The design variables of TF was calculated using EM simulation, and the design variables of TF are shown in Table 1. Figure 4 (a) shows the schematic of the QAF, and the design variables are shown in Table 2. Figure 4. (b) shows the gilbert type analog adder that adds the I/Q signal.

TABLE 1 DESIGN PARAMETERS OF TF

	L1 [pH]	Q1	L2 [pH]	Q2	K
IN	144	10.4	413	6.6	0.65
OUT	291	16.1	169	3.5	0.48

TABLE 2 DESIGN PARAMETERS OF QAF

L 1,2 [pH]	C 1,2 [fF]	R 1,2,3,4 [ohm]	R 5,6 [ohm]
300	130	50	100

III. CONCLUSION

Figure 5 shows the measured gain and phase, RMS Gain Error and RMS Phase Error according to the 6-Bit input from 26.5 GHz to 29.5 GHz. The input loss and reflection loss are <15 dB, RMS phase error of $2.8\,^{\circ}$ - $3.3\,^{\circ}$, RMS gain error of $0.9\,\mathrm{dB} - 1.1\,\mathrm{dB}$, and 1dB compression point (P1dB) of $3.2\mathrm{dB}$ over 26.5 GHz to 29.5 GHz. The layout and microphotograph of the proposed phase shifter are shown in Figure 6. The core size is $562\mathrm{um} \times 454\mathrm{um}$.

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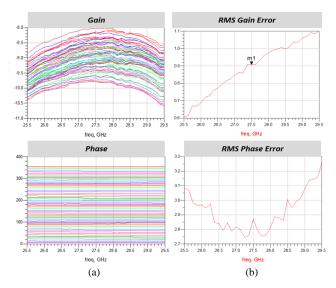


Fig. 5 (a) Measured gain and phase according to input bit (b) RMS gain and phase error

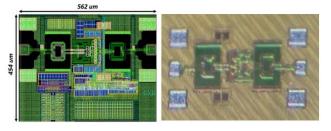


Fig. 6 Layout and microphotograph of proposed phase shifter

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