Prof. Tao HANG

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Dr. Tao HANG is currently a full professor at Shanghai Jiao Tong University (SJTU). He received his B.S. and Ph.D. from SJTU in 2004 and 2010, respectively. He has worked in the University of Michigan (U.S.), Waseda University (Japan), and Northwestern University (U.S.) as the visiting scholar and postdoctoral fellow for 5 years. He currently serves as the vice dean at the School of Materials Science and Engineering, and the director of the Institute of Electronic Materials and Technology at SJTU. His research interest mainly focused 3D packaging materials and technology (Cu interconnection, low temperature bonding), nanostructured materials and functional thin films fabricated by electrochemical method (electrodeposition, electro-grafting, electrochemical-etching). He has published more than one hundred academic papers in multiple high impact journals such as Nat. Electron., Sci. Adv., PNAS, Adv. Mater., Acta Mater., etc.

Title

Electrochemistry for High Performance Chip Interconnects

Abstract

The rapid development of information technology requires better performance of chips, for which the density of transistors and interconnects on chips is massively expanding. Electroplating is the main fabrication technique for the interconnection in damascene and packaging process, and the increase of interconnection density has put forward new requirements for the electrodeposition of interconnects. In this talk, the recent research progress regarding the electrodeposition and property regulation of chip interconnects will be introduced, including the filling and the post-processing of 3D through silicon via and damascene interconnects, electrodeposition and reliability of high density micro-bumps, preparation and application of interconnects with various particular structures, application of micro/nano cone array in low-temperature bonding and chemical/electrochemical grafting of organic insulating films. Hopefully these researches may bring the enlightenment and promote the development of high-density interconnection technology of chips.