

Circuit Design and Analysis for Error Suppression in Heavy-Hexagon Surface Codes

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Heavy Hexagon 구조에서 서피스 코드 오류 억제를 위한 회로 설계 및 분석

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Abstract

The structure and performance of quantum error correction codes are fundamentally shaped by qubit connectivity, which in solid-state quantum systems is constrained by planar lattices and further architectural limitations, leading to sparse interaction graphs such as the heavy-hexagon lattice used in current IBM Quantum devices. Under such limited connectivity, each qubit typically interacts with only two or three neighboring qubits, often requiring additional operations such as SWAP gates to mediate interactions. Using the Surface Code-17 as a representative example, we show that an optimized ordering of CNOT operations in stabilizer measurement circuits significantly reduces error propagation. Simulation results further validate the effectiveness of the proposed approach in suppressing error propagation in such lattice architectures.

I. Introduction

Fault-tolerant quantum computing requires scalable hardware with high-fidelity physical qubits to accommodate the large overhead of quantum error-correcting (QEC) codes, such as surface code [1,2].

While existing studies have demonstrated effective hook error mitigation in surface codes implemented on high-connectivity lattices, such approaches are not directly affordable to hardware architectures with constrained connectivity [3]. IBM Quantum devices adopt a heavy-hexagonal lattice with only two or three nearest neighbors per qubit to suppress crosstalk and gate errors [4]. This limited connectivity introduces additional circuit overhead, such as SWAP operations or auxiliary flag qubits [5], which complicates hook error suppression and increases the risk of error propagation.

In this paper, we redesign the ordering of CNOT operations in stabilizer measurement circuits implemented on the heavy-hexagon lattice to mitigate error propagation and validate its effectiveness through simulation.

II. SC-17 on the heavy-hexagon lattice

1. Hook error

A hook error (or horizontal hook error) is an error-propagation phenomenon in which a single physical fault is copied onto two data qubits, with the resulting correlated error occurring along the direction of a logical operator.

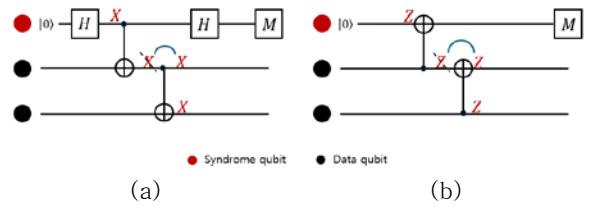


Fig.1 The circuit-level illustration of a hook error with (a) X error and (b) Z error

2. Proposed method

Our work is based on the IBM heavy-hex superconducting processor architecture, employing a depth-minimizing, SWAP-based “fold-unfold” embedding with bridge qubits [4]. Here, we assume that bridge qubits are used only for exchanging positions with data qubits, and that the information stored on them does not affect communication.

As illustrated in Fig. 2(a), the Surface Code-17 can be mapped onto the heavy-hexagon lattice by

stabilizing the data qubits over two successive sub-rounds. In each sub-round, a distinct subset of stabilizers is measured, as shown in Fig. 2(b).

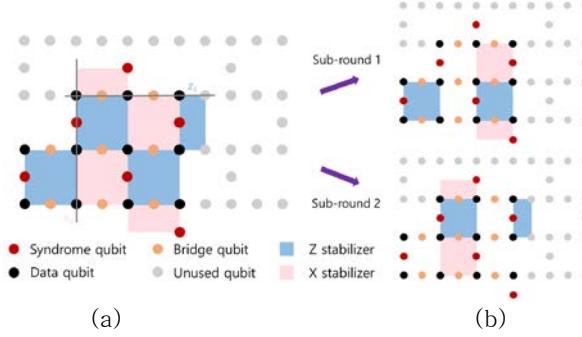


Fig.2 Embedding of the rotated surface code with $d=3$: Qubit arrangements (a) and the two sub-rounds with the stabilizers (b)

Here, we take sub-round 1 as an example (Fig. 3(a)). To mitigate the error propagation occurred in [5], we modify the ordering of CNOT operations in the embedding circuits. The key requirement is to ensure consistency of the output results after the exchange of data and bridge qubits.

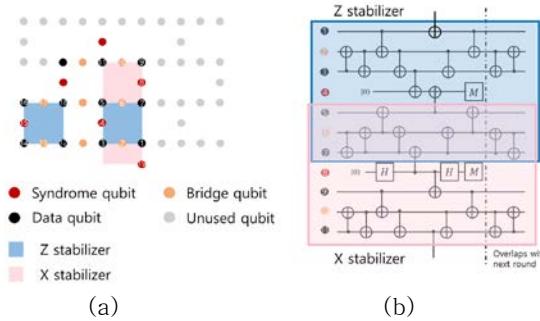


Fig.3 Sub-round 1 (a) and the proposed embedding circuit (b)

3. Simulation results

We implemented the standard depolarizing noise channel and Minimum Weight Perfect Matching(MWPM) decoder, which has been detailedly described in [6].

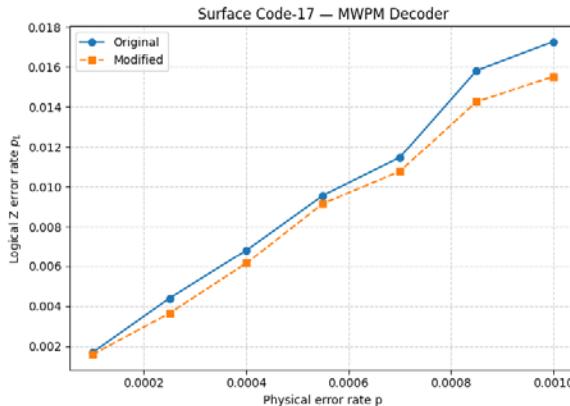


Fig.4 Comparison of logical Z error rates between our proposed approach and the original circuit in [5]

Fig. 4 shows that as the physical error rate increases, the logical error rate rises for both circuits, which is

consistent with expectations. However, across the entire range of physical error rates, the modified circuit consistently exhibits a lower logical Z error rate than the original circuit. This improvement is particularly noticeable, indicating that the optimized CNOT ordering effectively suppresses hook error so that prevents propagation. These results demonstrate that, even under the connectivity constraints of the heavy-hexagon architecture, careful redesign of the stabilizer measurement circuit can lead to a measurable enhancement in logical error performance.

III. Conclusion

In this paper, we proposed a new CNOT sequence for Surface Code-17 implemented on the heavy-hexagon lattice to mitigate potential hook errors. Simulation results showed that our proposed approach achieves a lower logical error rate under the MWPM decoder.

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