A Ramp-Triggered On-Time Switching in a 1-MHz GaN Based Bootstrap Gate Driver for Three-Level Buck Converters

Ihsan Ul Haq, Muhammad Awais, and Jong-Wook Lee
Department of Electronics and Information Convergence Engineering, Kyung Hee University

Abstract

The increasing electrification of vehicles demands compact and energy-efficient power converters capable of high speed operation at elevated power levels. To enhance power density, a GaN based bootstrap gate driver for a three-level buck converter operating at 1 MHz is proposed. The design regulates the bootstrap rail voltage (V_{BST}) through controlled bootstrap capacitor charging and incorporates deadtime control to prevent the shoot-through current. The system operates reliably with a 10 V input and is implemented in a 130 nm CMOS process.

I. Introduction

As EVs, renewable energy, and compact systems push for higher efficiency and power density, silicon-based three-level converters are approaching their limits. However, silicon MOSFETs and all NMOS stages offer low cost and ease of integration, but at the expense of inherent trade-offs among switching loss, conduction loss, and multi-MHz, high voltage designs. Recent wide-bandgap demonstrations [1], [2] highlight a shift toward multi-MHz, high power density solutions, motivating GaN as a replacement for silicon in advanced three-level topologies.

Compared with silicon MOSFETs, GaN devices offer lower gate charge and output capacitance, enabling higher switching frequencies with lower loss [1]. Their negligible reverse recovery reduces deadtime (t_{dead}) and improves commutation efficiency [4]. In three-level legs, GaN's superior figure-of-merit reduces conduction and switching losses, allowing smaller flying capacitors and inductors. Recent demonstrations confirm the suitability of GaN for compact, high-density converters [3].

However, silicon based three-level converters still face limitations that motivate a GaN-based design. The design in [5] achieves high integration but requires complex interception-coupling t_{dead} control and a three-switch bootstrap driver, which makes it sensitive to parasitics and limits scalability. Other silicon implementations operate at modest switching frequencies and require large passive components for ripple control, reducing power density. Overall, silicon three-level converters remain constrained in efficiency, passive size, and control complexity for multi-MHz, high-power-density targets.

To address these challenges, a proposed technique is implemented in Section II, while Section III concludes the paper.

II. Proposed design

The proposed GaN based bootstrap gate-driver architecture for the three-level buck converter is shown in Fig. 1. The power stage comprises four GaN switches (M_1, M_2, M_3, and M_4), and three bootstrap capacitors (C_{B1}, C_{B2}, and C_{B3}) supply the required high side gate drive voltages. When M_1 is conducting, M_2 and M_4 are off, whereas when M_2 is conducting, M_1 and M_3 remain off.

Bootstrap capacitor charging is controlled by PMOS switches (M_{P1}, M_{P2}, and M_{P3}), which connect each capacitor to its associated low side node only when the corresponding low-side GaN device is on. The switching node voltage V_{SW} is sensed and compared with a reference voltage V_{REF} to regulate the V_{SW} to $V_{IN}/2$. The resulting sensing voltage (V_S)

is compared with a ramp signal to generate a trigger for the on-time controller, which produces the high and low side control signals (V_H and V_L) with inserted t_{dead}, thereby generating the four gate-drive outputs (V_1, V_2, V_3, and V_4).

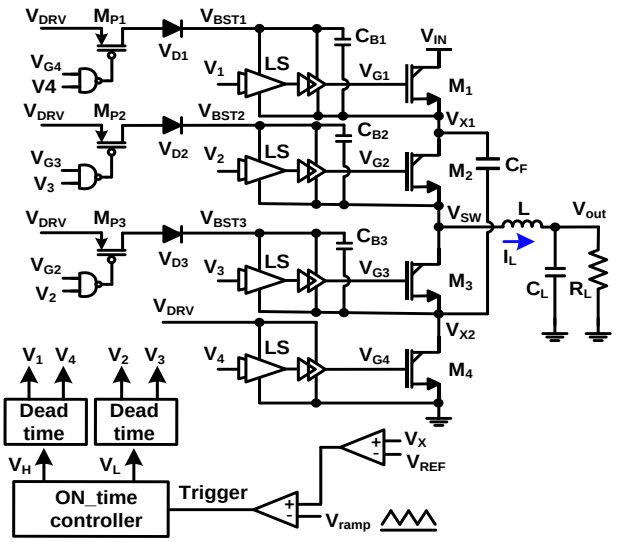

Fig. 1. Block diagram of the proposed system architecture.

Fig. 2 shows the simulated waveform of the proposed system. The gate drive voltages V_{G1}, V_{G2}, V_{G3} and V_{G4} correspond to the switching of M_1, M_2, M_3, and M_4, respectively. The node V_{X1} operates between V_{IN} and $V_{IN}/2$, while the V_{SW} and V_{X2} nodes operate between $V_{IN}/2$ and gnd. The inductor current waveform is shown with a peak value of approximately 278 μA.

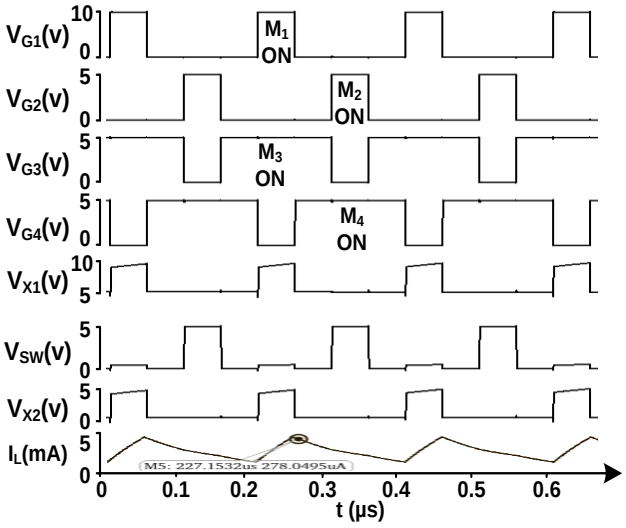

Fig. 2. Simulated waveform of GaN-based three-level buck converter.

Fig. 3 shows the power efficiency (η) as a function of current, with η = 87%.

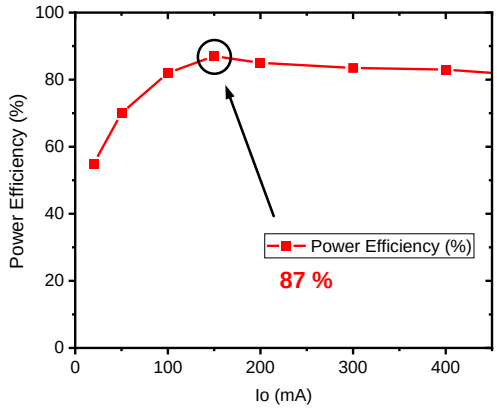

Fig. 3. Calculated efficiency of the converter.

III. Conclusion

A GaN-based bootstrap gate-driver for a three-level buck converter was presented. The design enables regulated bootstrap operation and reliable three-level switching at a frequency of 1 MHz, as verified by simulation results.

ACKNOWLEDGMENT

This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (No. RS-2024-00333296).

REFERENCES

[1] S. J. Lee, et al, "A design of a 100-MHz fully integrated digital pulse width modulation three-level buck converter using package bond-wire inductor," *IEEE Access*, vol. 13, pp. 50032–50042, 2025.

[2] Y. Zhong, "A review on the GaN-on-Si power electronic devices," *Fundamentals of Semiconductor Devices, vol. 2*, no. 3, pp. 100–123, 2022.

[3] Efficient Power Conversion (EPC), "How to design an ultra-thin, highly efficient, multi-level DC-to-DC converter using eGaN® FETs," How2AppNote 015, Application Note, 2019.

[4] S. Biswas and D. Reusch, "GaN-based switched capacitor three-level buck converter with cascaded synchronous bootstrap gate drive scheme," *in Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018.

[5] B. Lee and D. B. Ma, "A 20 MHz on-chip all-NMOS 3-level DC–DC converter with interception coupling dead-time control and 3-switch bootstrap gate driver," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 6339–6347, Jul. 2021.