A Two-Step, Cyclic Vernier-Based Time-to-Digital Converter Using Dynamic Element Matching

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요 약

This paper presents a two-step, cyclic vernier-based time-to-digital converter using dynamic element matching (DEM). The DEM is achieved by storing GRO's state in the previous conversion to be used as the beginning state of the next conversion. The signal propagation path in the two Vernier GRO is changed between two consecutive conversions and depends on the amount of time input. Therefore, the systematic error is randomized and achieving DEM. The prototype TDC is fabricated on a 180 nm CMOS process with a 0.0042 mm2 area. It achieved 50 ps resolution on the total 11-bit dynamic range with the maximum DNL and INL are 1.2 and 1.82 LSB, respectively. The power consumption is only 0.2 mW at the maximum conversion rate of 0.5 MS/s.

Ⅰ. Introduction

Time-to-digital converter (TDC) can be used to precisely measure and quantize the time interval between two input events into an output digital code. TDCs have been widely adopted in an all-digital phase-locked loop (ADPLL) for phase comparator as well as biomedical imaging applications to provide timing information. For an instant, in Time-of-Flight (ToF) Positron Emission Tomography (PET) imaging, many research efforts are devoted to integrating TDCs with an array of Single-Photon Avalanche Diodes (SPADs) on the same substrate and to build the novel digital Silicon Photomultiplier (dSiPM) in standard CMOS technology. The challenges of TDC design are high resolution and long-range timing as well as small area and low power as much as possible.

Previously, various types of TDC have been reported. The first ΔΣ noise shaping gated-ring oscillator based TDC architecture is reported in [1]. It achieved first order noise shaping and does not require an explicit feedback loop. However, it operates in a short range and suffers from the current leakage and dead-zone which degrade the output performance. In [2], a delay latch chain architecture is used for replacing the delay line and the sample register to reduce area. But with delay structure, the mismatch and process variation become a big issue by decreasing the linearity of the conversion. In addition, an ADC-based TDC in [3] achieve high resolution by passing through 2 steps: translates the time interval into the charge, and quantize the charge by an ADC. However, the area and power still large with a small dynamic range. A state-of-the-art TDC architecture based on cyclic interpolators also reported in [4] which can reach a high resolution and dynamic range even with and very old process 0.35um, but still consume large power and low conversion speed.

In this brief, we describe a GRO-based Vernier DEM TDC architecture is proposed. Two GROs oscillate at a slightly output frequency different and each corresponding internal phase of them is compared to each other to form a cyclic Vernier loop, allow extending the DR with less effort. The GRO's output phase is preserved after each conversion and become the beginning state of the next conversion. Hence, even though the buffer chain is fixed by the GRO loop, the signal propagation path is randomly changed by each consecutive conversion due to unknown and asynchronous time input. Thus, DEM is achieved.

Ⅱ. Design

Figure 1 illustrates the design of our prototype, in which the block diagram of the full system is shown. The input generator processes the input timing from the START/STOP signals and the other block's feedback to generate the enable signal to the GRO core block. The Phase generator and Clock generator generate the final data output of the TDC.

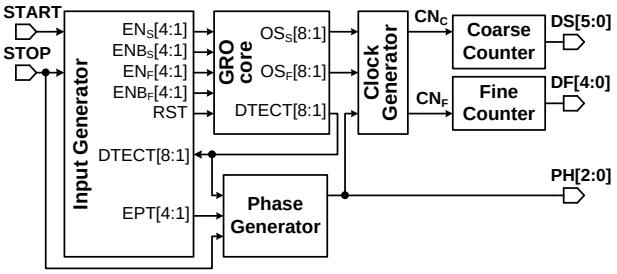

Figure 1. Proposed TDC architecture.

Figure 2(a) shows the design of the GRO core. It includes two differentials gated ring oscillator working at a small frequency difference and a comparator chain to detect the alignment event position. The oscillator state at the end of the conversion is stored, and it is the beginning state of the next conversion. Therefore, the signal propagation between different conversion is different; hence, the DEM is achieved. Figure 2(b) shows the circuit design of a delay stage of the GRO.

Figure 3 shows the measured of linearity characteristic of the behavioral model. A uniformly

distributed 2×10^6 time input in the full DR is injected into the TDC. The differential non-linearity (DNL) is obtained by counting the hits of each bin, and the integral non-linearity (INL) is obtained using the cumulative sum of DNL. The TDC achieves a DNL of 1.2 LSB (maximum) and 0.8 LSB_{rms}. The INL performance is 1.82 LSB (maximum) and 0.95 LSB_{rms}.

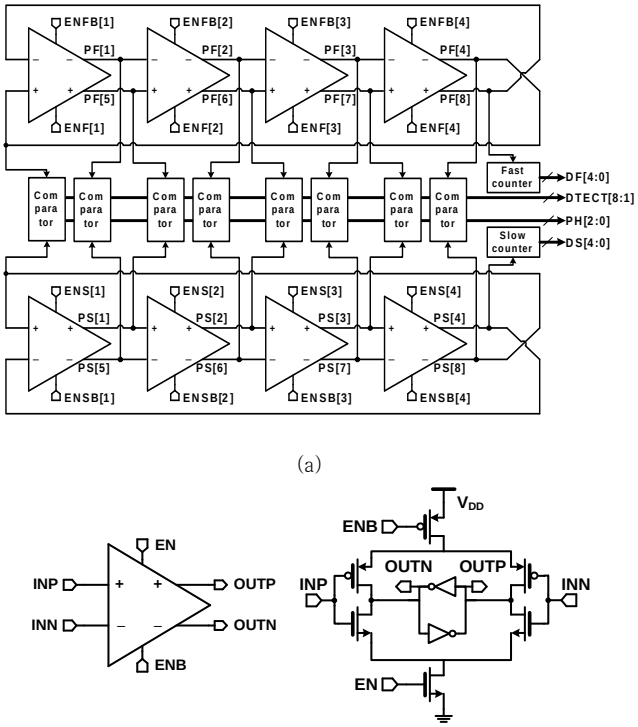

Figure 2. Block diagram of the GRO core

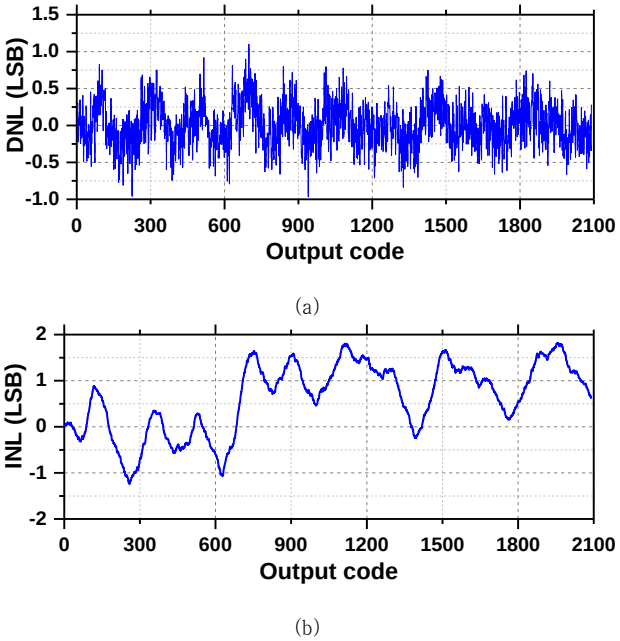

Figure 3. Measured of the TDC linearity. (a) DNL and (b) INL.

Figure 4 shows the measured transfer characteristic of the TDC. The resolution of a TDC is defined as the minimum time interval that a TDC can resolve, and it can be estimated as the reciprocal of the slope. From the linear fitting curve, we obtain a resolution of 50 ps.

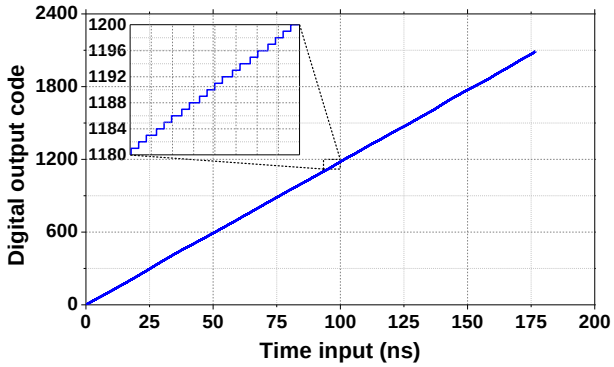

Figure 4. Measured TDC input/output characteristic.

Ⅲ. Conclusions

A wide range dynamic element matching TDC design has been presented. It is expected to have a wide dynamic range as depending on the counter size of the coarse step which can be changed easily in each application. The TDC is expected to achieve high resolution and linearity, which can be applied in various application such as phase comparator in a high-speed all-digital phase-locked loop; or integrated with an array of SPADs to build a fluorescence lifetime sensor for the biomedical application.

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참 고 문 헌

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